11.4 A 1V 17GHz 5mW Quadrature CMOS VCO based on Transformer Coupling

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Because of the demand for lower cost, lower power, and higher data rates in both wireless and wired communication systems, integrated circuits and systems are constantly pushed to higher operating frequencies and lower power consumptions. Furthermore, because of continuous device scaling and power-supply scaling for power reduction in digital circuits, the supply voltage used in mixed-signal systems also needs to be reduced. Therefore, a quadrature signal generator, as required for I/Q modulation and demodulation, should be able to operate at high frequency from a low supply voltage with low power consumption.

Two LC VCOs can be forced to oscillate in quadrature by using additional coupling transistors in parallel with the core negative-resistance transistors as demonstrated in [1]. However, this technique suffers from a compromise between quadrature accuracy, power consumption, and phase noise. As proposed in [2], the tradeoff can be relaxed by connecting the coupling transistors in series with the core negative-resistance transistors. However, in this case, the coupling transistors have to be five times larger than the negative resistance transistors [2], which would not only increase the loading and the power consumption but also reduce the operation frequency and the tuning range. Furthermore, connecting the coupling transistors in cascode fashion would increase the voltage headroom and make the circuit unsuitable for low supply voltages.

Figure 11.4.1 shows the schematic of the proposed transformer-coupled quadrature VCO (TC-QVCO). The varactors used for fine tuning and the switched-capacitor arrays (SCAs) used for coarse tuning are omitted for readability. Two tail-biased LC VCOs are cross-coupled by on-chip transformers, instead of by coupling transistors as in conventional LC-QVCOs, to generate quadrature signals. Each LC VCO is formed by a negative-resistance transistor and an LC tank. The structure is similar to the transformer-feedback VCO presented in [3], but here the transformer is used to cross-couple the two LC VCOs. The primary coil of each of the transformers (L_{p1a}) resonates with the total capacitance at the drain and, at the same time, is cross-coupled to the secondary coil (L_{s1a}) of the quadrature phase. As such, the parasitic loading capacitors contributed by the coupling transistors are removed, which results in higher operating frequency, larger tuning range, higher tank voltage, and lower phase noise. Furthermore, compared to conventional VCOs, the transformers enable the signals at the sources of the transistors to swing below the negative supply and thus effectively reduce the voltage headroom and the minimum supply voltage [3]. The tail current sources of the two VCOs are also shared for better IQ balance [4].

The proposed TC-QVCO is designed and fabricated in a 0.18µm CMOS process. The process has 6 metal layers with a 2µm-thick top metal. The threshold voltages of the PMOS and NMOS transistors are around 0.51V and -0.5V, respectively. Figure 11.4.2 shows the die micrograph of the fabricated chip. The TC-QVCO is fully integrated, with a total area of 0.37mm^2 including pads. Because the TC-QVCO is fully differential, two symmetrical center-taped transformers are used to implement (L_{p1a}, L_{p1b}, L_{s1a} and L_{s1b}) and (L_{p2a}, L_{p2b}, L_{s2a} and L_{s2b}) to minimize the chip area and to maximize the quality factor. Figure 11.4.3 shows the layout and the model of the transformers. The transformers are designed with turn ratios of 2:1 and are laid out using the top metal for maximum Q. The secondary coils are placed totally inside the primary coils in order to maximize the self-inductances for a given area. An octagonal shape is used to further enhance the quality factor.

The transformer is characterized as an individual test structure. The primary and secondary coil differential self-inductances are measured to be 656pH and 194pH with quality factors of 5.2 and 2.5, respectively. The coupling coefficient is 0.59. Accumulation-mode varactors implemented by placing NMOS devices in the n-well are used for fine tuning, and 2b SCAs are used for coarse tuning. Both the varactors and SCAs are optimized for maximum Q to avoid degrading the Q of the LC tank.

The phase noise of the TC-QVCO was measured with the Agilent E4448A spectrum analyzer with phase noise personality. The QVCO can be tuned between 14.8 and 17.6GHz, corresponding to a tuning range of 16.5%. The measured frequency spectrum and phase noise are shown in Figs. 11.4.4 and 11.4.5, respectively. The measured phase noise is -110dBc/Hz at 1MHz offset from the 17GHz carrier frequency. The QVCO draws only 5mA from a 1V power supply. The proposed TC-QVCO was also tested at the low supply voltages and can operate normally for a supply voltage as low as 0.6V. Figure 11.4.6 shows the phase noise plot with a 0.6V supply. The measured phase noises are -102.6dBc/Hz at 1MHz offset and -125.3dBc/Hz at 10MHz offset.

Operating at 17GHz and a 1V supply with 16.5% tuning range, the proposed QVCO achieved a figure of merit (FOM) of 187.6dB, which is defined as:

$$FOM = 10\log\left[\left(\frac{f_o}{\Delta f}\right)^2 \frac{1}{L(\Delta f)\times P_{diss}|_{mW}}\right]$$

and is comparable to other recently published QVCOs.

In order to measure the quadrature accuracy of the proposed TC-QVCO, the method of single-sideband (SSB) up-conversion has been chosen. The phase and amplitude errors of the QVCO, which are very difficult to measure directly and reliably at high operating frequencies, are translated into the sideband rejection, which measures the ratio of wanted sideband to the unwanted sideband. For this purpose, a scaled version of the TC-QVCO operating at 8.5GHz and an on-chip single-sideband mixer with inductive loading were implemented in a separate test structure. Figure 11.4.7 shows the up-converter frequency spectrum with a sideband rejection of 28dB. The unwanted sideband is caused by mismatches in the QVCO, the single-sideband mixer, and the baseband quadrature signals. Assuming that the phase mismatch from the TC-QVCO is dominant, a side-band rejection of 28dB is equivalent to a phase error of approximately 4.5°.

References:

[1] A. Rofougaran et al., "A 900MHz CMOS LC-Oscillator with Quadrature Outputs," *ISSCC Dig. Of Tech. Papers*, pp. 391-393, Feb., 1996.

[2] P. Andreani, "A Low-Phase-Noise Low-Phase-Error 1.8GHz Quadrature CMOS VCO," *ISSCC Dig. Of Tech. Papers*, pp. 290-292, Feb., 2002.

[3] K. Kwok, and H. C. Luong, "Ultra-Low-Voltage High-Performance VCO Using Transformer Feedback," *IEEE J. Solid-State Circuits*, Vol. 40, pp. 652-660, March, 2005.

[4] C. Lo and H. Luong, "2-V 900-MHz Quadrature Coupled LC Oscillators with Improved Amplitude and Phase Matching," *Proc. IEEE Symp. Circuits and Systems*, 1999, pp. 585–588.

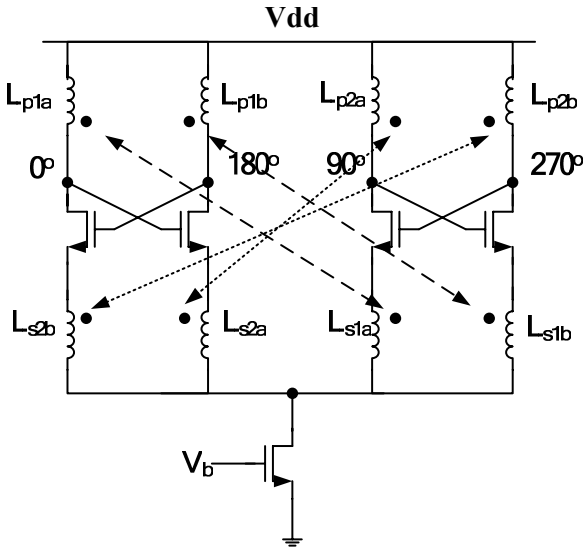

Figure 11.4.1: Schematic of the proposed transformer-coupled QVCO.

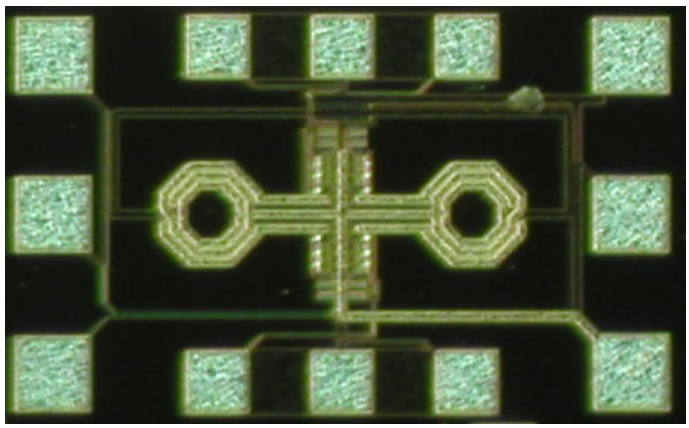

Figure 11.4.2: Die micrograph of the TC-QVCO (dimensions: 0.48mm x 0.78mm).

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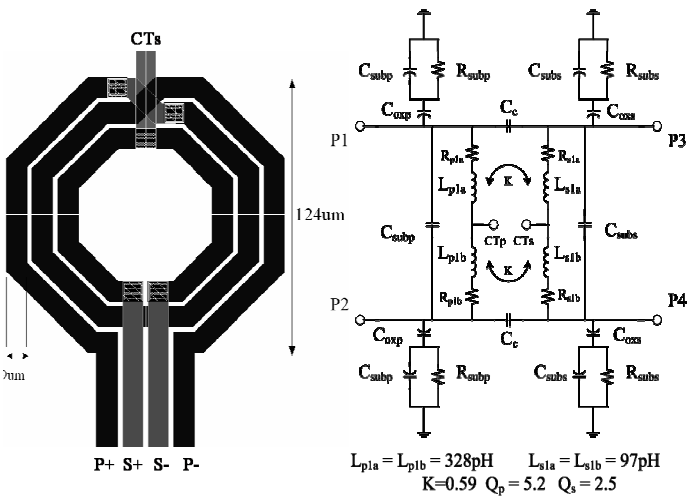

Figure 11.4.3: Transformer layout and model.

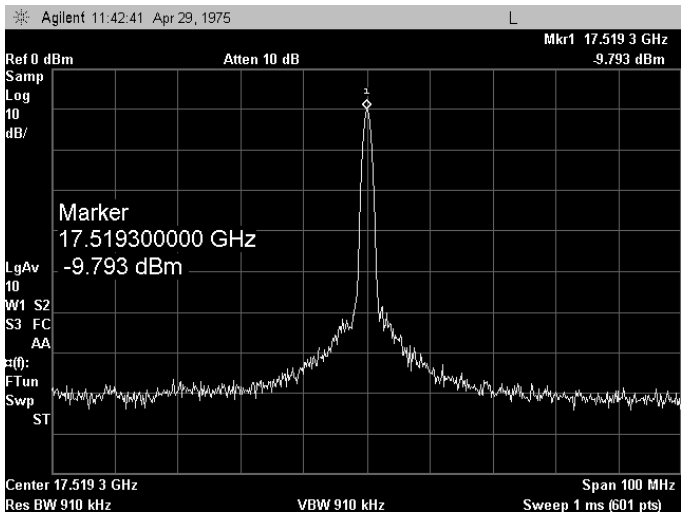

Figure 11.4.4: Frequency spectrum of the QVCO.

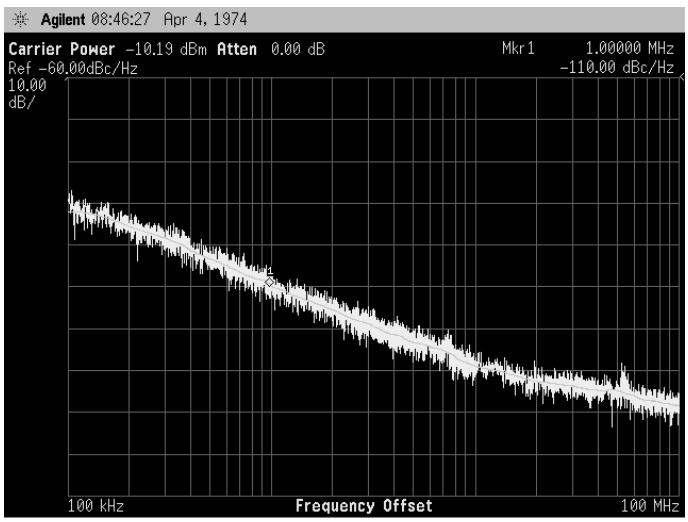

Figure 11.4.5: Phase noise plot of the QVCO at 1V supply.

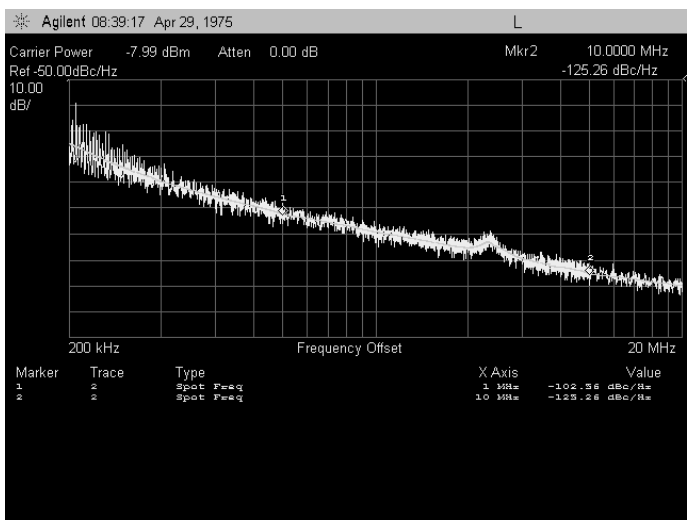

Figure 11.4.6: Phase noise plot of the QVCO at 0.6V supply.

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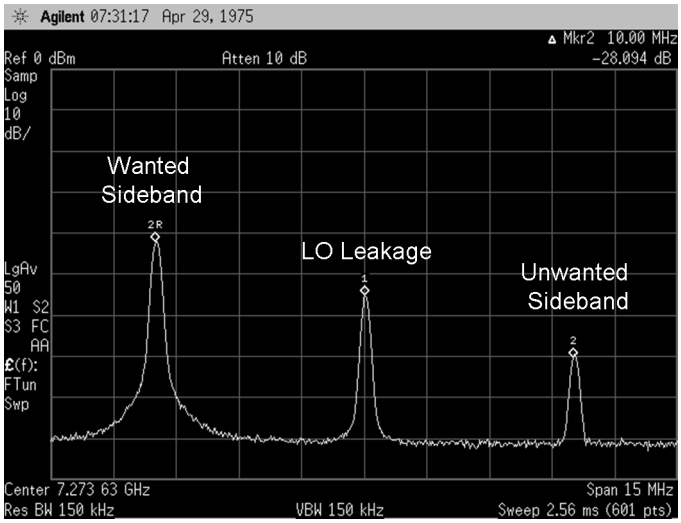

Figure 11.4.7: Upconverted baseband signals and LO leakage.

